WHAT IS CLAIMED IS:

1. A phase locked state detecting apparatus for detecting a phase locked state of a processing clock signal with respect to a reference clock signal, the processing clock signal generated by a phase locked loop and used in an information processing, the reference clock signal being the reference for control by the phase locked loop, the phase locked state detecting apparatus comprising:

a detecting device which detects a change of frequency of the processing clock signal and generates a detecting signal;

a determining device determines on the basis of the detecting signal whether or not the processing clock signal is in the phase locked state with respect to the reference clock signal.

2. The phase locked state detecting apparatus according to claim 1, wherein the detecting device comprises: a edge counter which counts an interval of a rising edge timing of the processing clock signal; and a processing unit regards the interval as a value indicating the frequency of the processing clock signal to detect the change of the frequency of the processing clock signal.

3. The phase locked state detecting apparatus according to claim 1, wherein the determining device determines on the basis of the detecting signal that the processing clock signal is in the phase locked state with

respect to the reference clock signal when the change of the frequency of the processing clock signal is less than a preset threshold value, and

determines that the processing clock signal is not in the phase locked state with respect to the reference clock signal when the change is not less than the threshold value.